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10CS74

Seventh Semester B.E. Degree Examination, Aug./Sept. 2020
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. What are the three classes of manstream computer and their characteristics **(03 Marks)**

b. How do you calculate the cost of an integrated circuit in terms of wafer diameter and Die area? **(07 Marks)**

c. Find the number of dies per 400 mm diameter wafer for a die that is 2cm on a side. **(08 Marks)**

d. Define module availability in terms of MTTFS and MTTR. **(02 Marks)**

2 a. How do you specify the performance of a computer? **(02 Marks)**

b. How do you specify the SPECRatio of a computer? **(04 Marks)**

c. Explain the utility of Amdahl's law. **(06 Marks)**

d. Suppose you want to achieve a speedup of 80 with 100 processors, what fraction of the original computation can be sequential. **(08 Marks)**

3 a. What is pipelining? **(02 Marks)**

b. What are the major hurdles of pipelining? **(06 Marks)**

c. Discuss how do you minimize data hazard stalls by forwarding. **(06 Marks)**

d. Explain delayed branch technique. **(06 Marks)**

4 a. Explain the two types of name dependencies. **(06 Marks)**

b. Discuss the advantages and disadvantages of Loop unrolling. **(06 Marks)**

c. Explain how you can overcome data hazard with dynamic scheduling with Tomasulo's approach. **(08 Marks)**

PART – B

5 a. Discuss hardware – based speculation in ILP. **(10 Marks)**

b. Describe the use of branch target buffer and the steps involved in handling an instruction with BTB. **(10 Marks)**

6 a. Gives Flynn's taxonomy of parallel architecture with examples. **(04 Marks)**

b. What are two classes of multiprocessors? **(06 Marks)**

c. What is multiprocessor cache coherence? **(04 Marks)**

d. Discuss two classes of protocols to track the sharing of a data block. **(06 Marks)**

7 a. What are the three categories of cache organization for block placement? (08 Marks)

b. Assume we have a computer where clocks per instruction CPI is 1.0 when all memory access hit the cache. The only data access are loads and stores, and these total 50% of the instructions. If the miss penalty is 25 clock cycles and the miss rate is 2%, how much faster would the computer be if all instruction were cache hits. (06 Marks)

c. Explain in brief what are the six basic cache optimizations. (06 Marks)

8 Write short notes on the following :

a. Dynamic branch prediction in ILP

b. Directory – based cache coherence protocol

c. Power equation of an integrated circuit

d. Handling exceptions in instruction pipeline. (20 Marks)

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